ABSTRACT

A disclosed processor includes update logic coupled to a register. The update logic receives a first signal indicative of a first add-compare-select (ACS) instruction result and a second signal indicative of a second ACS instruction result, and updates the contents of the register dependent upon the first and second signals. In the event the first and second signals are received substantially simultaneously, the update logic shifts the contents of the register 2 bit positions in order thereby vacating 2 consecutive bit positions, updates one of the vacated bit positions dependent upon the first signal, and updates the other vacated bit position dependent upon the second signal. A described method for decoding convolutional code includes generating computer program code for a processor including two or more ACS instructions. Storage elements specified by each of the ACS instructions are selected such that the processor can execute the ACS instructions substantially simultaneously.